Course : MCA Semester – IV

MICROPROCESSORS, INTERFACING AND APPLICATIONS

Subject Code : 17MCA4C23

**UNIT-1**

1. Intel 8086 is a \_\_\_\_\_\_\_ microprocessor.

**[a] 16-bit** [b] 32-bit [c] 8-bit [d] 64-bit

2. Intel 8086 microprocessor consists of \_\_\_\_\_\_ address lines.

[a] 16 **[b] 20**  [c] 24 [d] 32

3. Which one of the following is a control flag of 8086?

[a] Carry flag [b] Zero flag **[c] Direction flag** [d] Sign flag

4. BIU stands for \_\_\_\_\_\_\_\_\_\_\_\_\_.

[a] Bus Interactive Unit **[b] Bus Interface Unit**  [c] Bus Interrupt Unit

[d] Base Interface Unit

5. EU stands for \_\_\_\_\_\_\_\_\_\_\_\_.

**[a] Execution Unit** [b] Elementary Unit [c] Enable Unit [d] Extended Unit

6. Which one of the following is a segment register?

[a] BP [b] SP **[c] SS** [d] SI

7. The 8086 microprocessor consists of \_\_\_\_\_\_\_ segment registers.

**[a] 4** [b] 3 [c] 2 [d] 8

8. DS is referred to as \_\_\_\_\_\_ register.

[a] Decode Segment [b] Divide Segment [c] Digital Segment **[d] Data Segment**

9. DI is a \_\_\_\_\_\_\_\_\_ register.

[a] pointer **[b] index** [c] data [d] base

10. The Instruction Pointer is \_\_\_\_\_\_ in length.

**[a] 16 bits** [b] 20 bits [c] 8 bits [d] 12 bits

11. The size of a memory segment of 8086 is \_\_\_\_\_\_.

[a] 64 MB [b] 2 MB [c] 1 MB **[d] 64 KB**

12. The 8086 fetches instructions from the \_\_\_\_\_\_\_ segment of the memory.

[a] stack **[b] code** [c] extra [d] data

13. The 8088 microprocessor consists of a \_\_\_\_\_\_\_\_\_ instruction queue.

[a] 6-byte **[b] 4-byte** [c] 3-byte [d] 5-byte

14. The functions of pins \_\_\_\_\_\_\_ depend on the mode in which 8086 is operating.

**[a] 24-31** [b] 22-29 [c] 14-21 [d] 16-23

15. If MN/MX is low the 8086 microprocessor operates in \_\_\_\_\_\_\_\_ mode.

[a] intermediate **[b] minimum** [c] maximum [d] min-max

16. The 8086 microprocessor supports \_\_\_\_\_\_ types of instruction formats.

**[a] 6** [b] 4 [c] 8 [d] 12

17. The 8088 microprocessor consists of a \_\_\_\_\_\_\_\_\_ data lines.

[a] 16 [b] 20 **[c] 8** [d] 12

18. DEN stands for \_\_\_\_\_\_\_\_\_.

[a] Direct Enable [b] Direct Encode [c] Data Encode **[d] Data Enable**

19. MOV AX, BX is an example of \_\_\_\_\_\_\_\_\_\_\_ addressing instruction.

[a] direct [b] indirect [c] immediate  **[d] register**

20. Which one of the following registers is used in I/O addressing?

**[a] DX**  [b] AX [c] CX [d] BX

21. The \_\_\_\_\_\_\_\_\_ is a set of conductors that connects the CPU to its memory and I/O devices.

**[a] system bus** [b] I/O bus [c] memory bus [d] data bus

22. The addressing capacity of Intel 8086 microprocessor is \_\_\_\_\_\_\_\_\_\_.

[a] 64 MB [b] 2 MB **[c] 1 MB** [d] 64 KB

23. The current status of the processor is stored in a register called \_\_\_\_\_\_\_\_\_\_.

[a] program status word [b] instruction register

[c] status register  **[d] processor status word**

24. Intel 8086 microprocessor consists of \_\_\_\_\_\_ conditional flags and \_\_\_\_\_\_ control flags.

**[a] 6, 3** [b] 4, 5 [c] 3, 6 [d] 5, 4

25. In register indirect addressing the effective address of the operand is in the \_\_\_\_\_ register.

[a] DX [b] AX [c] CX **[d] BX**

**UNIT-2**

1. The correct assembler instruction format of 8086 is:

**[a] Label : Mnemonic Operand, Operand ; Comments**

[b] Mnemonic Operand, Operand : Comments ; Label

[c] Comments; Label : Mnemonic Operand, Operand

[d] Mnemonic Operand, Operand : Label ; Comments

2. The instruction LEA stands for \_\_\_\_\_\_\_\_\_\_\_.

[a] Label Effective Address **[b] Load Effective Address**

[c] Load Extended Address [d] Label Extended Address

3. For a MOV DST, SRC instruction, the destination cannot be \_\_\_\_\_\_\_\_.

[a] memory [b] register **[c] immediate**  [d] direct

4. The CWD instruction extends the sign of the word in \_\_\_\_\_ to DX thus forming a double word.

[a] DX **[b] AX**  [c] CX [d] BX

5. The \_\_\_\_\_\_\_ instruction finds the 2’s complement of an operand.

[a] XOR [b] CMP [c] NOT **[d] NEG**

6. The MUL BL instruction multiplies the content of \_\_\_\_\_ by the content of BL.

[a] AX **[b] AL**  [c] CL [d] BX

7. The DIV CL instruction places the remainder in \_\_\_\_\_\_\_ register.

[a] AX [b] AL **[c] AH**  [d] CL

8. The instruction DAA stands for \_\_\_\_\_\_\_\_\_\_\_.

**[a] Decimal Adjust for Addition** [b] Data Adjust for Addition

[c] Decimal Adjust for Accumulator [d] Data Adjust for Accumulator

9. The instruction JP OPR means \_\_\_\_\_\_.

[a] Branch if not Positive [b] Branch on Odd Parity

[c] Branch on Positive **[d] Branch on Even Parity**

10. The LOOP OPR instruction \_\_\_\_\_\_\_\_\_\_.

**[a] checks the CX register** [b] checks the BX register

[c] checks the AX register [d] checks the DX register

11. The CLC instruction \_\_\_\_\_\_\_\_\_\_.

[a] clears CX register **[b] clears carry flag**

[c] clears CL register [d] clears CH register

12. The CMC instruction \_\_\_\_\_\_\_\_\_\_.

[a] complements CX register [b] compares carry flag

**[c] complements carry flag** [d] complements CL register

13. The STD instruction \_\_\_\_\_\_\_\_\_\_.

[a] stores data into a register [b] sets data into register

[c] store temporary data **[d] sets the direction flag**

14. The CLI instruction \_\_\_\_\_\_\_\_\_\_.

[a] Clear Logical Instruction **[b] Clears Interrupt flag**

[c] Clear Instruction [d] Compare Logical Instruction

15. The STC instruction \_\_\_\_\_\_\_\_\_\_.

**[a] Sets Carry flag** [b] Store Carry flag

[c] Store Tag for Carry [d] Set Time Clock

16. The NOT OPR instruction \_\_\_\_\_\_\_\_\_\_.

[a] finds 2’s complement of OPR [b] clears the content of OPR

**[c] finds 1’s complement of OPR** [d] complements output register OPR

17. Which one of the following operations is performed during TEST instruction?

[a] OR **[b] AND** [c] XOR [d] NOT

18. In the instruction SHR OPR, the destination OPR can have any of the 8086 addressing modes except the \_\_\_\_\_\_\_\_\_ mode.

**[a] immediate**  [b] indirect [c] implied [d] direct

19. In the instruction ROL OPR, CNT, the value of CNT must be 1 or \_\_\_\_\_\_\_\_.

[a] CX [b] CH **[c] CL** [d] 0

20. Which one of the following registers is true with RCL instruction?

[a] Reverse Carry Left [b] Rotate CL register

[c] Rotate Carry Left **[d] Rotate left through carry**

21. The instruction MOVSB \_\_\_\_\_\_\_\_\_.

**[a] moves byte string**  [b] moves bit string [c] Moves BX [d] Moves BL

22. Which one of the following instructions affects condition flags?

[a] LODSB [b] STOSB **[c] SCASB** [d] LODSW

23. The REP Prefix repeatedly executes the specified string instruction until \_\_\_\_.

**[a] CX = 0**  [b] CH = 0 [c] CL **= 0** [d] CF = 0

24. Which one of the following instructions is correct?

[a] ADC AX, AL [b] ADC AH, AX **[c] ADC AX, BX** [d] ADC BX

25. The LODSB instruction loads the content of content of SI into \_\_\_\_\_\_ register.

[a] AX **[b] AL** [c] AH [d] BL